STITCHED MICRO-VIA TO ENHANCE ADHESION AND MECHANICAL STRENGTH

Abstract of the Disclosure

A method for forming a via in an integrated circuit packaging substrate includes embedding an interfacial adhesion layer at a base of a via, and heating the materials at the base of the via. Embedding the interfacial adhesion layer further includes placing a conductive material over the interfacial adhesion layer. An interfacial layer material is deposited within at the base of opening and a conductive material is placed over the interfacial material. The interfacial layer material is a material that will diffuse into the conductive material at the temperature produced by heating the materials at the base of the via opening. Heating the materials at the base of the via opening includes directing energy from a laser at the base of the opening. An integrated circuit packaging substrate includes a first layer of conductive material, and a second layer of conductive material. The integrated circuit packaging substrate also includes a via for interconnecting the first layer of conductive material and the second layer of conductive material having a base that includes an interfacial adhesion material to stitch the base of the via to a layer of circuitry.

"Express Mail" mailing label number: EV 332568811 US
Date of Deposit: September 25, 2003
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